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EXAMINER	
GOSSAGE, GLENN A	

ART UNIT	PAPER NUMBER
2187	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,083	SADE ET AL.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2003 and 12 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 12-41* is/are rejected.

7)☒ Claim(s) *8-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The abstract of the disclosure is objected to because it does not enable one to quickly determine from a cursory inspection the nature and gist of the technical disclosure as required by 37 CFR 1.72(b). It appears one or two sentences should be added describing additionally claimed and disclosed features. [For example, in line 8, after "memories.", insert one or two sentences such as --First and second access balancing techniques may be used for data accessed from the cache memories, which may comprise disk data and control data, such as data indicating whether data in the caches has been modified and is write pending.--. See claims 4-5 and page 8, line 18 to page 9, line 21, for example.] Also, in line 7, it appears ":" (the colon) should be changed to --at least one of-- for clarity and consistency (note claim 11, e.g.).

Appropriate correction is required. See MPEP § 608.01(b).

2. The proposed drawing corrections filed December 19, 2003 have been approved by the Examiner, subject to drafting review.

However, the proposed substitute or replacement sheets of drawings filed December 19, 2003 have been DISAPPROVED by the Examiner. The proposed "replacement" sheets show changes marked in blue ink (similar to the annotated sheets), include extraneous marks such as the various "X" marks used to show the deletion of a numeral or label (see proposed replacement sheets 1/10 and 2/10, e.g.), and include labels for steps in the flowcharts which are not within the "boxes" or "diamonds" for those steps (note proposed replacement sheets 4/10 and 6/10, e.g.).

Applicant is REQUIRED to submit corrected substitute or replacement sheets of drawings in response to this Office action. Corrections to the drawings will not be held in abeyance.

3. The drawings are also objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first hardware" and "second hardware" (within the "specialized hardware" of claim 25, and the "third hardware" and "fourth hardware" (within the "specialized hardware") of claim 26, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

In this regard, applicants' arguments filed December 19, 2003 have been considered but are not persuasive.

The argument that the "specialized hardware" shown in Figure 14 constitutes the first hardware, second hardware, third hardware and fourth hardware is not persuasive because the drawings must show every feature as claimed. Since applicants choose to individually claim the first, second, third and fourth hardware (as opposed to the "specialized hardware" performing the functions), the individual hardware (circuits) as claimed should be shown so that it is clear to what each of the first, second, third and fourth hardware refers, and so that one may determine what equivalents there might be to each of the first, second, third and fourth hardware.

4. It is once again noted that the disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

On page 9, in the paragraph beginning on line 10, at line 11 of the paragraph, "is" appears to read more clearly here as --must be--. In line 13 of the (amended) paragraph, it appears --cache-- should be inserted before "memories" for clarity and consistency.

On page 19, in the paragraph beginning on line 7, at line 12 of the paragraph, it appears "associate" should be --associated-- for clarity.

On page 21, in the paragraph beginning on line 19, at line 6 of the paragraph, the wording (or through) "some means (not shown)" is vague and indefinite. [Note that this issue was not addressed by way of either amendment or argument, in the responses filed 12-19-03 and 04-12-04.]

On page 22, in the paragraph beginning on line 5, at line 2 of the paragraph, the reference to "a queue length" is unclear in this context since no "queue length" appears to have been discussed in the specification and is not adequately clear to what "queue length" is being referred to in this instance.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

The specification is also objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The specification does not describe or otherwise provide antecedent basis for any "machine executable code" for implementing the steps or acts as claimed. The specification also does not appear to describe a computer program product which is "stored on a computer readable medium" as now claimed.

In this regard, applicants' arguments filed December 19, 2003 have been considered but are not persuasive. Initially, the argument that the antecedent support may be found in the Summary of the Invention at page 4, lines 1-8 is not persuasive since antecedent support for the invention as claimed should be provided in the Detailed Description of the Invention, as it relates to the other parts of the disclosure such as the drawings, not merely as part of the Summary of the Invention. Moreover, the cited portion in the Summary of the Invention, while providing some antecedent support for claims such as claims 19 and 31, does not provide antecedent support for claims such as claims 22, 27-28 and 32-41, by way of example only.

In the claims:

In claim 12, line 2, it appears --first and second-- should be inserted before "cache" for consistency (see claim 1, line 7 and claim 14, lines 2-3, e.g.).

In claim 14, line 2, the wording "requests for (the) cache memories" is not clear as it is not readily apparent how a cache itself is "requested?" [Should --data stored in-- or --data from-- be inserted after "for" for clarity and consistency? Note the language of claim 1, line 6, e.g.]

In claim 16, line 2, it appears "said" (second occurrence) should be deleted for clarity.

In claim 32, line 2, it appears --selecting-- should be inserted after "for" for clarity and consistency (note claim 31, line 8, e.g.).

In claim 33, line 2, it appears ", further" should be deleted.

Appropriate correction is required.

5. Claims 19-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19, and therefore its dependent claims, as well as claim 20, the proper antecedent for "the requested data" is not entirely clear (see claim 18, lines 6 and 8, and claim 19, line 3, e.g.). Moreover, it is not entirely clear when the second access balancing technique would be used since the condition ("in response to a request for data that is stored in both the first cache memory and the second cache memory") is the same as in claim 18 (see claim 18, lines 6-9).

In claim 22, it is not entirely clear how this claim further limits claim 20 as this limitation would appear to be encompassed within the language of claim 18, lines 6-9 and claim 19, lines 3-6. [In this regard, also see 37 CFR 1.75(b) and (c) and 35 U.S.C. 112, fourth paragraph.]

In claim 25, it is not adequately clear to what the "first hardware" and "second hardware," which are within the "specialized hardware," refer in this instance. The terms and phrases used

in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (in this regard, see also 37 CFR 1.75(d)(1)).

Similarly, in claim 26, it is not adequately clear to what the "first hardware" and "second hardware," which are within the "specialized hardware," refer here.

In this regard, applicants' arguments filed December 19, 2003, insofar as applicable, have been considered but are not persuasive.

With respect to claim 19 and the second access balancing technique, the examiner recognizes that the machine executable code may select a cache memory in accordance with a second access balancing technique. However, it is not clear from the claim language how the access balancing technique selection is performed since the condition or trigger ("in response to a request for data that is stored in both the first cache memory and the second cache memory") is the same. [Should --first-- and --second-- be inserted before "request" in claim 18, line 6 and claim 19, line 3, respectively?]

With respect to claim 22, the argument that claim 22 further limits the claims by reciting that the cache selection hardware and machine executable code each implements at least one of the first and second access balancing techniques (response at page 15) is not persuasive since this language would appear to be encompassed within the language of claim 18 (which affirmatively sets forth that the cache selection hardware selects one of the cache memories in accordance with a (first) accessing balancing technique) and claim 19 (which affirmatively sets

forth that the machine readable code selects one of the cache memories in accordance with a second access balancing technique). See claim 18, lines 6-9 and claim 19, lines 1-2, as well as claim 19, lines 3-6. The intended scope and meaning of claim 22, in addition to claims 19 and 20 thus becomes unclear. [Again in this regard, see also 37 CFR 1.75(b) and (c) and 35 U.S.C. 112, fourth paragraph.]

With respect to claims 25and 26, the argument that because the specification describes the "specialized hardware" which provides the functionality described in conjunction with Figs. 9-13, it is adequately clear to what the first, second, third and fourth hardware refer (response at page 15), is also not persuasive. Where is the "first (second, third, fourth) hardware" described at all in the specification? Does each of the first, second, third and fourth hardware correspond to one of the chips? If the "specialized hardware" is on a single chip, does each of the first, second, third and fourth hardware correspond to a part of the single chip? The specification does not appear to give adequate guidance as to what the first, second, third and fourth hardware refer here. If one cannot ascertain, with a reasonable degree of certainty, to what the first (second, third, fourth) hardware refers, one is also not able to determine what equivalents there might be to each of the hardware elements. Again, the terms and phrases used in the claims MUST find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (in this regard, see also 37 CFR 1.75(d)(1)).

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 31-41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification as originally filed does not appear to provide an adequate written description of a computer program product which is "stored on a computer readable medium" (the computer program product could be on a carrier wave or transmitted via some other medium and need not necessarily be "stored on a computer readable medium" as now claimed).

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 4-7, 12-32 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dewey et al in view of Kurokawa et al.

With respect to claim 1, as well as claims 18 and 31, Dewey et al discloses a method and system for managing data in a cache, the system including a first cache memory including data (cache 20 in Figure 1, e.g.) and a second cache memory including data (cache 21), wherein at least some of the data included in the first cache memory is the same as at least some of the data of the second cache memory (see column 5, lines 34-52). However, Dewey et al does not teach providing cache selection hardware for selecting, in response to a request for data that is stored in

both the first cache memory and the second cache memory, which one of the first and second cache memories to use to obtain the data in accordance with an access balancing technique.

Kurokawa et al discloses a method and system for managing data in a redundant storage configuration, the system including first and second memories (storage devices S0 and S1), wherein at least some of the data of the first cache memory is the same as at least some of the data of the second cache memory (see column 4, lines 34-39 and 54-63, e.g.). Kurokawa et al further teaches, in response to a request for data that is stored in both the first cache memory and the second cache memory, choosing which one of the cache memories to use to obtain the data according to an "access balancing" technique (see column 2, lines 55-67 and column 5, line 67 to column 6, line 4, e.g.) so as to even out or balance accesses between the storage devices. [While

Kurokawa et al does not state that the storage devices S0 and S1 are themselves "cache" storage devices, Kurokawa et al teaches that they may include some "cache" storage (see column 9, line 62 to column 10, line 10, e.g.]

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to select or choose which one of the memories in Dewey et al to use to obtain data in response to a request for data that is stored in both the first cache memory and the second cache memory, because Kurokawa et al teaches that performance of a data storage system storing redundant data may be improved by evening out or balancing accesses to two (or more) storage devices storing the same data.

Also with respect to claim 31, as well as claims 19 and 21-28, one of ordinary skill in the art would readily recognize that computer related inventions may be implemented in software or hardware, and the selective use of software or a "computer program product," or a combination of hardware and software, to implement the method and system of Dewey et al in view of Kurokawa et al as previously discussed, would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made and, as such, does not render the claimed invention patentably distinct.

With respect to claims 2 and 7, as well as claims 23-24 32 and 37, Kurokawa et al discloses that the access balancing technique may include selection using an interleaving technique so that the memories are alternately accessed. In this manner, the memories may be accessed in a "round robin" manner.

With respect to claim 4, as well as claims 16, 20 and 34, Dewey et al discloses that the data may include "control data" such as status data indicating whether the data is "dirty" or modified,

as well as corresponding disk data. Kurokawa et al also teaches storing data indicative of the status the data in the memories.

With respect to claims 5 and 6, as well as claims 35 and 36, access to both the control data and disk data stored in Dewey et al may be balanced in light of the teachings of Kurokawa et al, i.e. the same balancing technique may be used for the control data and disk data.

With respect to claims 12-15 and 17, Kurokawa et al teaches that the selection of the cache memories may utilize circuitry which may be considered to be "specialized" hardware, and that the "specialized" hardware may include at least one chip or integrated circuit (see column 19, lines 48-53, e.g.).

With respect to claims 29 and 30 (dependent from claim 29?), Dewey et al teaches providing first and second buses (see buses 18A and 18B) coupled to the first and second cache memories and associated controllers, similar to the first and second buses shown in applicants' Figure 1A.

8. Claims 3 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dewey et al in view of Kurokawa et al as applied to claims 1-2, 4-7, 12-32 and 34-37 above, and further in view of Mason et al.

With respect to claim 3, as well as claim 33, Dewey et al in view of Kurokawa et al discloses a method for managing data in a data storage system including balancing access to first and second cache memories which store common data (see number paragraph 8 above), but does not teach that the access balancing technique is based on statistics including monitoring a number of accesses of the memories over a predetermined amount of time and selecting one of the cache memories based on the access frequencies.

Mason et al similarly discloses a data storage system including a plurality of memories storing mirrored data, and additionally teaches dynamically adjusting a mirror service policy by collecting statistics regarding accesses to the memories over a period of time in order to more evenly balance loading within the storage system (see page 2, lines 23-35 and page 6, lines 5-27, as well as claims 1-3 and 7, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to provide an access balancing technique in a mirrored storage system, which access technique is based on statistics, as taught by Mason et al, in the mirrored storage system of Dewey et al in view of Kurokawa et al, in order to more evenly balance loading the data storage system.

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-2, 4-7, 12 -32 and 34-37 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-35 of U.S. Patent No. 6,591,335 or claims 1-19 of U.S. Patent No. 6604,171, each taken separately, in view of Kurokawa et al.

With respect to claim 1, as well as claims 18 and 31, U.S. Patent No. 6,591,335 or U.S. Patent No. 6604,171, each taken separately, discloses a method for managing data in a cache including providing a first cache memory including data and a second cache memory including data, wherein at least some of the data included in the first cache memory is the same as at least some of the data of the second cache memory (see claims 1 and 17 of U.S. Patent 6,591,335 and claims 1, 5 and 14 of U.S. Patent 6,604,171, e.g.), but does not teach providing cache selection hardware for selecting, in response to a request for data that is stored in both the first cache memory and the second cache memory, which one of the first and second cache memories to use to obtain the data in accordance with an access balancing technique.

Kurokawa et al discloses a method and system for managing data in a redundant storage configuration, the system including first and second memories (storage devices S0 and S1), wherein at least some of the data of the first cache memory is the same as at least some of the data of the second cache memory (see column 4, lines 34-39 and 54-63, e.g.). Kurokawa et al further teaches, in response to a request for data that is stored in both the first cache memory and

the second cache memory, choosing which one of the cache memories to use to obtain the data according to an "access balancing" technique (see column 2, lines 55-67 and column 5, line 67 to column 6, line 4, e.g.) so as to even out or balance accesses between the storage devices. [While Kurokawa et al does not state that the storage devices S0 and S1 are themselves "cache" storage devices, Kurokawa et al teaches that they may include some "cache" storage (see column 9, line 62 to column 10, line 10, e.g.]

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to select or choose which one of the memories in U.S. Patent No. 6,591,335 or U.S. Patent No. 6604,171, each taken separately, to use to obtain data in response to a request for data that is stored in both the first cache memory and the second cache memory, because Kurokawa et al teaches that performance of a data storage system storing redundant data may be improved by evening out or balancing accesses to two (or more) storage devices storing the same data. Since applicants' present claims "read on" the resulting structure and method, the present claims would have been obvious, within the meaning of 35 U.S.C. 103.

Also with respect to claim 31, as well as claims 19 and 21-28, one of ordinary skill in the art would readily recognize that computer related inventions may be implemented in software or hardware, and the selective use of software or a "computer program product," or a combination of hardware and software, to implement the method and system of U.S. Patent No. 6,591,335 or U.S. Patent No. 6, 604,171, each taken separately, in view of Kurokawa et al as previously discussed, would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made and, as such, does not render the claimed invention patentably distinct.

With respect to claims 2 and 7, as well as claims 23-24 32 and 37, Kurokawa et al discloses that the access balancing technique may include selection using an interleaving technique so that the memories are alternately accessed. In this manner, the memories may be accessed in a "round robin" manner.

With respect to claim 4, as well as claims 16, 20 and 34, U.S. Patent No. 6,591,335 or U.S. Patent No. 6604,171, each taken separately, discloses that the data may include "control data" such as status data indicating whether the data is "dirty" or modified, as well as corresponding disk data (see . Kurokawa et al also teaches storing data indicative of the status the data in the memories.

With respect to claims 5 and 6, as well as claims 35 and 36, access to both the control data and disk data stored in U.S. Patent No. 6,591,335 or U.S. Patent No. 6604,171, each taken separately, may be balanced in light of the teachings of Kurokawa et al, i.e. the same balancing technique may be used for the control data and disk data.

With respect to claims 12-15 and 17, Kurokawa et al teaches that the selection of the cache memories may utilize circuitry which may be considered to be "specialized" hardware, and that the "specialized" hardware may include at least one chip or integrated circuit (see column 19, lines 48-53, e.g.).

With respect to claims 29 and 30 (dependent from claim 29?), the use of first and second buses coupled to the first and second cache memories to obtain separate access to the cache memories in the system of U.S. Patent No. 6,591,335 or U.S. Patent No. 6604,171, each taken separately, in view of Kurokawa et al, as discussed above would have been further readily

obvious to one of ordinary skill in the art at the time the claimed was made and does not render the claimed invention patentably distinct.

Claims 3 and 33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-35 of U.S. Patent No. 6,591,335 or claims 1-19 of U.S. Patent No. 6604,171, each taken separately, in view of Kurokawa et al, as applied to claims 1-2, 4-7, 12-32 and 34-37 above, and further in view of Mason et al.

With respect to claim 3, as well as claim 33, U.S. Patent No. 6,591,335 or U.S. Patent No. 6604,171, each taken separately, in view of Kurokawa et al, discloses a method for managing data in a data storage system including balancing access to first and second cache memories which store common data (see above), but does not teach that the access balancing technique is based on statistics including monitoring a number of accesses of the memories over a predetermined amount of time and selecting one of the cache memories based on the access frequencies.

Mason et al similarly discloses a data storage system including a plurality of memories storing mirrored data, and additionally teaches dynamically adjusting a mirror service policy by collecting statistics regarding accesses to the memories over a period of time in order to more evenly balance loading within the storage system (see page 2, lines 23-35 and page 6, lines 5-27, as well as claims 1-3 and 7, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to provide an access balancing technique in a mirrored storage system, which access technique is based on statistics, as taught by Mason et al, in the

mirrored storage system of U.S. Patent No. 6,591,335 or U.S. Patent No. 6604,171, each taken separately, in view of Kurokawa et al, in order to more evenly balance loading the data storage system.

10. Claims 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Applicants' arguments filed December 19, 2003 and April , 2004 have been considered but are not persuasive. It is believed applicants' arguments have been addressed in the preceding paragraphs.

Also, with respect to the prior art, the argument that Kurokawa et al "appears silent with regard to taking any action in response to a request for data stored in the first and second cache memories" and that Kurokawa et al "does not disclose or suggest choosing a cache memory to use to obtain the requested data when the data is stored in the first and second cache memories" (response filed December 19, 2003, at page 37) is not persuasive since Kurokawa et al is not silent with regard to taking action in response to a request for data stored in the first and second cache memories and in particular, Kurokawa et al teaches choosing or selecting a cache memory to use to obtain the requested data when the data is stored in the first and second cache memories. In short, applicants' arguments are not commensurate in scope with the claim language.

Kurokawa et al teaches, at column 2, lines 55-64, for example, that in a data storage having first and second memories containing at least some common or duplicate data, in response to a request for data which is stored in both of the first and second memories (see column 2, lines 56-61 of Kurokawa et al and also note claim 1, lines 6-7), selecting which one of the cache memories to use to obtain the requested data in accordance with an "access balancing" technique (see column 2, lines 58-66 of Kurokawa et al and note claim 1, lines 7-8). Here, Kurokawa et al teaches that a "workload" can be "averaged" between the separate storage devices storing duplicate data, which storage device "workload averaging" may be considered to be a storage device "access balancing" technique. Thus, it is respectfully submitted that the broad claim language "in response to a request ... choosing which ... of the cache memories to use ... in accordance with an access balancing technique" is met by the teachings of Kurokawa et al. Note also that Kurokawa et al further teaches that the storage devices which store duplicate data may be cache memories (see column 9, lines 62-65 and column 10, lines 6-9, e.g.). Moreover, Kurokawa et al teaches that overall higher throughput may be contained for a data storage having first and second memories storing duplicate data which utilizes such an "access balancing" technique in response to requests (see column 1, lines 60-62; column 2, lines 3-6 and 65-67; and column 20, lines 45-48, e.g.). The evening out of the workload of storage devices in a redundant storage configuration and overall higher throughput taught by Kurokawa et al provide ample motivation and suggestion to utilize an "access balancing" technique in a data storage having first and second memories storing at least some duplicate data, such as in Dewey et al, or Sade, to arrive at a structure and method on which applicants broad claims read. Therefore, the

invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the combined teachings of the references.

12. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187